IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (original) A method comprising:

defining a pair of spaced apart floating gates over a substrate;

forming a stacked control gate over each floating gate; and

forming a drain and a pair of sources by implantation using said stacked control gates as a mask.

2. (original) The method of claim 1 including using said control gates to protect said floating gates from said implantation.

3. (original) The method of claim 1 including self aligning said sources and drain to both of said control gates.

4. (original) The method of claim 1 including using substrate hot electron injection to charge said floating gates.

5. (previously presented) The method of claim 1, wherein defining a pair of spaced apart floating gates over a substrate includes,

forming the spaced apart floating gates over a triple well defined within the substrate.

6. (previously presented) The method of claim 1, wherein the pair of spaced apart floating gates are composed of polysilicon.

7. (previously presented) The method of claim 1, wherein the control gate is composed of polysilicon.

8. (previously presented) The method of claim 1, wherein the drain and the pair of sources are formed contemporaneously.

9. (new) A method for forming a pair of memory cells capable of functioning as non-volatile memory cells, comprising:

defining a pair of spaced apart floating gates over a substrate;

forming a stacked control gate over each floating gate; and

forming a drain and a pair of sources by implantation using said stacked control gates as a mask, so that substrate electrons are supplied from one of the pair of sources of a first memory cell through an underlying channel of a second memory cell along a path from the one of the pair of sources to the underlying channel, wherein a width of the path is greater than a width of one of the pair of memory cells.

10. (new) The method of claim 9 including using said control gates to protect said floating gates from said implantation.

11. (new) The method of claim 9 including self aligning said sources and drain to both of said control gates.

12. (new) The method of claim 9 including using substrate hot electron injection to charge said floating gates.

13. (new) The method of claim 9, wherein defining a pair of spaced apart floating gates over a substrate includes,

forming the spaced apart floating gates over a triple well defined within the substrate.

14. (new) The method of claim 9, wherein the pair of spaced apart floating gates are composed of polysilicon.

15. (new) The method of claim 9, wherein the control gate is composed of polysilicon.

16. (new) The method of claim 9, wherein the drain and the pair of sources are formed contemporaneously.